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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/008,497	01/16/98	INDUE	H 0433700547

MM4270230

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EXAMINER

RAGU S

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 09/30/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/008,497	Applicant(s) Inoue, Hiroyuki
	Examiner Steven Rao	Group Art Unit 2814

Responsive to communication(s) filed on Apr. 16, 1998.

This action is **FINAL**.

Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

Claim(s) 1-20 is/are pending in the application.

Of the above, claim(s) 10-20 is/are withdrawn from consideration.

Claim(s) _____ is/are allowed.

Claim(s) 1-9 is/are rejected.

Claim(s) _____ is/are objected to.

Claims _____ are subject to restriction or election requirement.

Application Papers

See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

The drawing(s) filed on _____ is/are objected to by the Examiner.

The proposed drawing correction, filed on _____ is approved disapproved.

The specification is objected to by the Examiner.

The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

All Some* None of the CERTIFIED copies of the priority documents have been received.

received in Application No. (Series Code/Serial Number) 08/747,928.

received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

Notice of References Cited, PTO-892

Information Disclosure Statement(s), PTO-1449, Paper No(s). 5

Interview Summary, PTO-413

Notice of Draftsperson's Patent Drawing Review, PTO-948

Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

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DETAILED ACTION

Specification

1. This application (substitute specification) does not contain an abstract of the disclosure as required by 37 CFR 1.72(b). An abstract on a separate sheet is required.
2. 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are:

Page 1, line 8 'a' is missing before, "MOS transistor".

Page 12, Lines 16-19, the thickness of polycrystalline film 13 is defined as one third of the distance between two portions of silicon oxide film 12. Applicant does not indicate what two portions (there are several portions of the silicon oxide film 12) applicant is referring to, thus making the whole sentence unclear.

Page 12, line 28-29, the polycrystalline silicon film 8 is processed to have a pattern which is separated on the silicon oxide film 4. Again this sentence is unclear.

Applicant in line 29 states a separation width without clarifying what is a separation width.

Applicant in line 30 describes a slit 10 a of figure 3 G, however figure 3 G has no reference to an element (slit) 10 a therein.

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Page 13 lines 1-3 again a separation width of film 8 is described without explaining what is a separation width. The entire three lines are unclear and do not further describe/clarify the last few sentences of page 12 which appears to be the applicant's intention. Correction is required. Applicant's cooperation is sought to correct the numerous errors in the specification.

Claim Rejections - 35 U.S.C. § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Chiu (U.S. Patent No. 4,994,402, herein after Chiu) or Matthews (U.S. Patent No. 5,134,083, herein after Matthews).

With respect to claim 1, Chiu discloses a method of manufacturing a semiconductor device with a buried conductive layer connected to the source and drain of a MOS transistor and extends over the gate electrode of the MOS transistor , the method includes the following steps:

Forming a gate oxide (insulating film) on a semiconductor surface.

Forming a Poly silicon film (first conductive layer) as a gate electrode and a psg (second insulating film) on the first insulating film.

Forming a third insulting film on the whole surface.

Selectively etching away the third insulating film (Col.1, lines 47-52 formation of Spacer oxide).

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Diffusing impurities in the exposed portions (Col.1, line 50).

Forming a second conductive film (Col.1 line 50-55).

Forming first mask layer and patterning it. (Col.1, lines 47-52).

Forming a second mask layer , selectively etching it to leave a pattern (Col.2, lines 61-

64).Matthews in cols. 2 and 3 also discloses the above method steps.

With respect to claim 2, Matthews in fig. 20 A and Chiu in fig. 13 disclose a mask layer on an insulating film and also a mask on a conductive film.

With respect to claim 3, the recitation of forming two mask layers on an insulating film does not patentably distinguish it over cited art.

With respect to claim 4, it recites a mask layer on an insulating film and a mask layer on a conductive film and essentially opposite of the claim 2 recitation and therefore is rejected over Matthews disclosure in Fig.20 A and Chiu in fig.13, as also stated under claim 2 above.

With respect to claim 5, Chiu in Col. 7, lines 20 -25 and Matthews in figs.16 to 18 disclose two mask layers formed of a conductive film.

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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4. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu or Matthews as applied to claims 1-5 above, and further either in view of Kwon et al. (U.S. Patent No. 5,073,510 herein after Kwon).

With respect to claim 6, in addition to the disclosure of Chiu or Matthews stated under claim 1, they (Chiu or Matthews) disclose all steps of claim 6 except forming the wiring layer that is connected to the second conductive film at the bottom of the contact hole. However Kwon in the entire Col. 5 discloses forming a contact hole and forming the wiring layer that is connected to the second conductive film at the bottom of the contact hole. One skilled in the art at the time the invention was made would be motivated to combine the references as stated above to reduce the thickness of the protective oxide layer and to improve the bend of the chip.

With respect to claim 7, in addition to the disclosure of Chiu and Matthews as stated above under claim 1 and the combination of either with Kwon as stated under claim 6 above, Kwon in col.5, lines 40-53 discloses the coating of a conductive film and forming a fourth conductive film and processing it (fourth conductive film) into an electrode pattern.

With respect to claim 8, in addition to the disclosure stated under claims 1 and 6 above Kwon discloses the steps of coating a conductive film with a dielectric film, forming a dielectric film thereon and processing it (the dielectric film formed on the dielectric coated conductive film) to form an electrode.

With respect to claim 9, in addition to the disclosure stated under claim 8 above, Kwon in cols. 4 and 5 discloses the step of coating a mask layer with a dielectric film.

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8. The prior art made of record and not relied upon in this office action but is considered pertinent to applicant's disclosure are U.S. Patent Nos.: 4,689,869; 4,997,790; 5,115,296 and 5,340,761 all of these patents describe methods of forming submicron MOS transistors.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The fax number is (703) 308-7722 or -7724. The Examiner can be normally reached on Monday-Friday from 9.00 a.m. to 6.00 p.m. (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor (SPE) Olik Chaudhuri, can be reached at (703) 306-2794.

10. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission at the above mentioned fax numbers.

11. Any inquiry of a general nature or relating to the status of this application should be directed to the Technology center 2800 receptionist at (703) 308-0956.

September 13,1999.

